In the Claims:

Claims 1-35 were pending at the time of the Office Action.

Claims 1-29 and 32-35 are allowed.

Claims 30 and 31 stand rejected under 35 USC 103.

Please cancel claims 30 and 31 without prejudice.

The claim listing is as follows:

1. (Original) A multifunction peripheral device comprising:

a printer system;

a scanner system;

an input/output (IO) system;

a processor system; and,

a switch fabric for routing packet-based data between the printer system, the scanner system, the IO system, and the processor system through switch IO buses, the switch IO buses providing a point-to-point dedicated interconnection between the switch fabric and each of the printer system, the scanner system, the IO system, and the processor system.

2. (Original) A multifunction peripheral device as recited in claim 1, wherein each system is integrated onto a distinct application specific integrated circuit (ASIC).

3. (Original) A multifunction peripheral device as recited in claim 1, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the printer system and the scanner system which permits the transfer of packet-based data directly between the printer system and the scanner system.

4. (Original) A multifunction peripheral device as recited in claim 1, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the printer system and the IO system which permits the transfer of packet-based data directly between the printer system and the IO system.

5. (Original) A multifunction peripheral device as recited in claim 1, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the printer system and the processor system which permits the transfer of packet-based data directly between the printer system and the processor system.

6. (Original) A multifunction peripheral device as recited in claim 1, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the scanner system and the IO system which permits the transfer of packet-based data directly between the scanner system and the IO system.

7. (Original) A multifunction peripheral device as recited in claim 1, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the scanner system and the processor system which permits the transfer of packet-based data directly between the scanner system and the processor system.

8. (Original) A multifunction peripheral device as recited in claim 1, further comprising a switch IO bus providing a point-to-point dedicated

interconnection between the processor system and the IO system which permits the transfer of packet-based data directly between the processor system and the IO system.

9. (Original) A multifunction peripheral device as recited in claim 1, further comprising:

one or more enhanced IO ports; and,

a switch IO to PCI bridge which couples the switch fabric to the one or more enhanced IO ports through a switch IO bus providing a point-to-point dedicated interconnection between the switch fabric and the bridge, and through a PCI bus providing an interconnection between the bridge and each one of the one or more enhanced IO ports.

10. (Original) A multifunction peripheral device as recited in claim 1, further comprising:

one or more enhanced IO ports; and,

a second switch fabric for routing packet-based data between the one or more enhanced IO ports and the switch fabric through switch IO buses, the switch IO buses providing point-to-point dedicated interconnections between each of the one or more enhanced IO ports and the second switch fabric, and between the second switch fabric and the switch fabric.

11. (Original) A printer comprising:

a printer system;

an IO system;

a processor system; and,

a switch fabric for routing packet-based data between the printer system, the IO system, and the processor system through switch IO buses, the switch IO buses providing a point-to-point dedicated interconnection between the switch fabric and each of the printer system, the IO system, and the processor system.

12. (Original) A printer as recited in claim 11, wherein each system is integrated onto a distinct ASIC.

13. (Original) A printer as recited in claim 11, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the printer system and the IO system which permits the transfer of packet-based data directly between the printer system and the IO system.

14. (Original) A printer as recited in claim 11, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the printer system and the processor system which permits the transfer of packet-based data directly between the printer system and the processor system.

15. (Original) A printer as recited in claim 11, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the processor system and the IO system which permits the transfer of packet-based data directly between the processor system and the IO system.

16. (Original) A printer as recited in claim 11, further comprising:

one or more enhanced IO ports; and,

a switch IO to PCI bridge which couples the one or more enhanced IO ports to the switch fabric, each of the one or more enhanced IO ports coupled to the bridge through a PCI bus, and the bridge coupled to the switch fabric through a point-to-point dedicated switch IO bus.

17. (Original) A printer as recited in claim 11, further comprising:

one or more enhanced IO ports; and,

a second switch fabric for routing packet-based data between the one or more enhanced IO ports and the switch fabric through switch IO buses, the switch IO buses providing point-to-point dedicated interconnections between each of the one or more enhanced IO ports and the second switch fabric, and between the second switch fabric and the switch fabric.

18. (Original) A multifunction peripheral device comprising:

a processor system integrated onto a processor ASIC;

an IO system integrated onto an IO ASIC;

two or more functional systems, each functional system for performing a peripheral function of the multifunction peripheral device, and each functional system integrated onto a distinct ASIC; and,

a switch fabric for routing packet-based data between the processor system, the IO system, and each of the functional systems through switch IO buses, the switch IO buses providing point-to-point dedicated interconnection between the switch fabric and the processor system, the switch fabric and the IO system, and the switch fabric and each of the functional systems.

19. (Original) A multifunction peripheral device as recited in claim 18, further comprising a switch IO bus providing a point-to-point dedicated

interconnection between the processor system and the IO system which permits the transfer of packet-based data directly between the processor system and the IO system.

20. (Original) A multifunction peripheral device as recited in claim 18, further comprising a switch IO bus between each of the one or more functional systems providing a point-to-point dedicated interconnection for transferring packet-based data directly between each of the one or more functional systems.

21. (Original) A multifunction peripheral device as recited in claim 18, further comprising a switch IO bus between each of the one or more functional systems and the processor system providing a point-to-point dedicated interconnection for transferring packet-based data directly between each of the one or more functional systems and the processor system.

22. (Original) A multifunction peripheral device as recited in claim 18, further comprising a switch IO bus between each of the one or more functional systems and the IO system providing a point-to-point dedicated interconnection for transferring packet-based data directly between each of the one or more functional systems and the IO system.

23. (Original) A multifunction peripheral device as recited in claim 18, further comprising:

one or more enhanced IO ports; and,

a switch IO to PCI bridge which couples the one or more enhanced IO ports to the switch fabric, each of the one or more enhanced IO ports coupled to

the bridge through a PCI bus, and the bridge coupled to the switch fabric through a point-to-point dedicated switch IO bus.

24. (Original) A multifunction peripheral device as recited in claim 18, further comprising:

one or more enhanced IO ports; and,

a second switch fabric for routing packet-based data between the one or more enhanced IO ports and the switch fabric through switch IO buses, the switch IO buses providing point-to-point dedicated interconnections between each of the one or more enhanced IO ports and the second switch fabric, and between the second switch fabric and the switch fabric.

25. (Original) A peripheral device comprising:

a processor system integrated onto a processor ASIC;

an IO system integrated onto an IO ASIC;

a peripheral system integrated onto a distinct peripheral ASIC for performing a peripheral function of the peripheral device; and,

a switch fabric for routing packet-based data between the processor system, the IO system, and the peripheral system through switch IO buses, the switch IO buses providing point-to-point dedicated interconnection between the switch fabric and the processor system, the switch fabric and the IO system, and the switch fabric and the peripheral system.

26. (Original) A peripheral device as recited in claim 25, further comprising a switch IO bus providing a point-to-point dedicated interconnection between the processor system and the IO system which permits

the transfer of packet-based data directly betwcen the processor system and the IO system.

27. (Original) A peripheral device as recited in claim 25, further comprising a switch IO bus between the peripheral system and the processor system providing a point-to-point dedicated interconnection for transferring packet-based data directly between the peripheral system and the processor system.

28. (Original) A peripheral device as recited in claim 25, further comprising a switch IO bus between the peripheral system and the IO system providing a point-to-point dedicated interconnection for transferring packet-based data directly between the peripheral system and the IO system.

29. (Original) A peripheral device as recited in claim 25, further comprising:

one or more enhanced IO ports; and,

a switch IO to PCI bridge which couples the one or more enhanced IO ports to the switch fabric, each of the one or more enhanced IO ports coupled to the bridge through a PCI bus, and the bridge coupled to the switch fabric through a point-to-point dedicated switch IO bus.

30. (Canceled)

31. (Canceled)

32. (Original) A method for transferring packet-based data within the intra-system architecture of a multifunction peripheral device comprising:

transmitting a request packet to a switch fabric from a processor system over a first dedicated switch IO bus;

forwarding the request packet to a printer system over a second dedicated switch IO bus;

generating a response packet at the printer system;

transmitting the response packet to the switch fabric from the printer system over the second dedicated switch IO bus; and,

forwarding the response packet to the processor system over the first dedicated switch IO bus.

33. (Original) A method as recited in claim 32, further comprising:

acknowledging receipt of any packet by the switch fabric and by any system.

34. (Original) A method as recited in claim 32, wherein the request packet is a first request packet and the response packet is a first response packet, the method further comprising:

transmitting a second request packet to the switch fabric from a scanner system over a third dedicated switch IO bus;

forwarding the second request packet to an IO system over a fourth dedicated switch IO bus;

generating a second response packet at the IO system;

transmitting the second response packet to the switch fabric from the IO system over the fourth dedicated switch IO bus; and,

forwarding the second response packet to the scanner system over the third dedicated switch IO bus.

35. (Original) A method as recited in claim 34, wherein the transmitting and forwarding of the first request packet and the first response packet happens concurrently with the transmitting and forwarding of the second request packet and the second response packet.